IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Lee**	§	Group Art Unit: **2185**
	§	
Serial No.: **10/814,733**	§	Examiner: **Campos, Yaima**
	§	
Filed: **March 31, 2004**	§	Attorney Docket No.: **AUS920040057US1**
	§	
For: **Data Processing System and Computer Program Product for Support of System Memory Addresses with Holes**	§	

35525
PATENT TRADEMARK OFFICE
CUSTOMER NUMBER

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

RESPONSE TO OFFICE ACTION

Sir:

No fees are believed to be required. If, however, any fees are required, I authorize the Commissioner to charge these fees which may be required to IBM Corporation Deposit Account No. 09-0447. No extension of time is believed to be necessary. If, however, an extension of time is required, the extension is requested, and I authorize the Commissioner to charge any fees for this extension to IBM Corporation Deposit Account No. 09-0447.

In response to the Office Action of May 2, 2006, please amend the above-identified application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 8 of this paper.

Amendments to the Specification:

Please amend the paragraph that starts on page 13, line 14, and ends on page 14, line 2, as follows:

It is important to note that while the present invention has been described in the context of a fully functioning data processing system, those of ordinary skill in the art will appreciate that the processes of the present invention are capable of being distributed in the form of a computer readable medium of instructions and a variety of forms and that the present invention applies equally regardless of the particular type of signal bearing media actually used to carry out the distribution. Examples of computer readable media include recordable-type media, such as a floppy disk, a hard disk drive, a RAM, CD-ROMs, or DVD-ROMs~~, and transmission-type media, such as digital and analog communications links, wired or wireless communications links using transmission forms, such as, for example, radio frequency and light wave transmissions~~. The computer readable media may take the form of coded formats that are decoded for actual use in a particular data processing system.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method of supporting memory addresses with holes, the method comprising the computer implemented steps of:

virtualizing a first physical address range allocated for system memory for an operating system run by a processor configured to support logical partitioning to produce a first logical address range;

virtualizing a second physical address range allocated for system memory for the operating system to produce a second logical address range, wherein the first physical address range and the second physical address range are non-contiguous and the first logical address range and the second logical address range are contiguous; and

virtualizing a memory mapped input/output physical address range that is intermediate the first physical address range and the second physical address range to produce a third logical address range, wherein a lowermost logical address of the third logical address range exceeds a respective uppermost ~~upper most~~ logical address of the first and second logical address ranges.

2. (Original) The method of claim 1, wherein the steps of virtualizing the first physical address range, the second physical address range, and the memory mapped input/output physical address range comprises maintaining a mapping table that defines physical addresses and corresponding logical addresses.

3. (Original) The method of claim 2, wherein maintaining the mapping table further comprises maintaining the mapping table in a physical address space allocated to one of the first and second physical address ranges, and wherein the physical address space is unavailable to an operating system accessing the first and second physical address ranges.

4. (Original) The method of claim 1, wherein the third logical address range is non-contiguous with the first logical address range and the second logical address range.

5. (Original) The method of claim 1, further comprising:

allocating a portion of at least one of the first physical address range and the second physical address range for a logical partitioning management software layer.

6. (Original) The method of claim 1, wherein the memory mapped input/output physical address range is allocated for cache inhibited addresses.

7. (Currently amended) A computer program product that is stored in a computer readable medium for virtualizing non-contiguous physical memory ranges into a contiguous logical address range, the computer program product comprising:

instructions for virtualizing a first range of contiguous physical addresses, which are allocated for system memory for an operating system run by a processor configured to support logical partitioning, to produce a first range of contiguous logical addresses;

instructions for virtualizing a second range of contiguous physical addresses, which are allocated for system memory for the operating system, to produce a second range of contiguous logical addresses, the first range of contiguous physical addresses and the second range of contiguous physical addresses being non-contiguous, the first range of contiguous logical addresses and the second range of contiguous logical addresses being contiguous and forming a combined range of contiguous logical addresses; and

instructions for virtualizing a third range of contiguous physical addresses, which is allocated for memory mapped input/output, that is intermediate to the first range of contiguous physical addresses and the second range of contiguous physical addresses to produce a third range of contiguous logical addresses, a lowermost logical address of the third range of contiguous logical addresses exceeding an uppermost logical address of the combined range of contiguous logical addresses.

~~first instructions for storing logical-to-physical memory address translations for first and second non-contiguous physical address ranges of a memory device allocated for system memory and a third physical address range comprising a memory mapped input/output physical address range that is intermediate the first and second physical address ranges, and wherein a lower-most logical address of the third physical address range provided by the logical-to-physical memory address translations is greater than an upper-most logical address of first and second logical address ranges provided by the logical-to-physical memory address translations corresponding to the first and second non-contiguous physical address ranges; and~~

~~second instructions, responsive to execution of the first instructions, for converting a logical address into a corresponding physical address.~~

8. (Currently amended) The computer program product of claim 7, further comprising instructions for maintaining a mapping table that defines physical addresses and their corresponding logical addresses. ~~wherein the logical-to-physical memory translations are stored in a mapping table that is unavailable to an operating system accessing the memory device.~~

9. (Currently amended) The computer program product of claim 8, wherein the mapping table is maintained in at least one of the first range of contiguous physical addresses and the second range of contiguous physical addresses. ~~and second physical address ranges.~~

10. (Currently amended) The computer program product of claim 7, further comprising instructions for converting a logical physical address into a corresponding physical address.
~~wherein the second instructions provide logical partitioning functionality.~~

11. (Currently amended) The computer program product of claim 7, further comprising:
instructions for converting a logical physical address into a corresponding physical address; and
the instructions for converting a logical physical address into a corresponding physical address being maintained in at least one of the first range of contiguous physical addresses and the second range of contiguous physical addresses.
~~wherein the second instructions are maintained in at least one of the first and second physical address ranges.~~

12. (Currently amended) The computer program product of claim 7, wherein the third range of contiguous logical addresses and the combined range of contiguous logical addresses are non-contiguous.
~~wherein the second instructions interface an operating system with input and output devices of a data processing system.~~

13. (Currently amended) The computer program product of claim 12, further comprising:
instructions for allocating a portion of at least one of the first range of contiguous physical addresses and the second range of contiguous physical addresses for a logical partitioning management software layer.
~~wherein the second instructions present a contiguous logical address range comprising the first and second logical address ranges to the operating system.~~

14. (Currently amended) The computer program product of claim 7 [[8]], wherein the third range of contiguous physical addresses ~~address range~~ is allocated for cache inhibited memory mapped input/output addresses.

15. (Currently amended) A data processing system for supporting non-contiguous system memory ranges ~~arrays~~, comprising:

a memory that contains a first range of contiguous physical addresses allocated for system memory, a second range of contiguous physical addresses allocated for system memory, and a third range of contiguous physical addresses allocated for memory-mapped input/output, the third range of contiguous physical addresses intermediate to the first range of contiguous physical addresses and the second range of contiguous physical memory addresses;

the first range of contiguous physical addresses and the second range of contiguous physical addresses being non-contiguous;

a processor for virtualizing the first range of contiguous physical addresses to produce a first range of contiguous logical addresses;

the processor for virtualizing the second range of contiguous physical addresses to produce a second range of contiguous logical addresses;

the first range of contiguous logical addresses and the second range of contiguous logical addresses being contiguous and forming a combined range of contiguous logical addresses; and

the processor for virtualizing the third range of contiguous physical addresses to produce a third range of contiguous logical addresses, a lowermost logical address of the third range of contiguous logical addresses exceeding an uppermost logical address of the combined range of contiguous logical addresses.

~~first and second non-contiguous physical memory arrays allocated for system memory having respective first and second physical address ranges and a third physical memory array having a third physical address range intermediate the first and second physical address ranges, a data set, and a set of instructions; and~~

~~a processor configured to support logical partitioning, wherein the processor, responsive to execution of the instructions, is presented with a contiguous logical address range for accessing the first and second non-contiguous memory arrays.~~

16. (Currently amended) The data processing system of claim 15, further comprising a data set, wherein the data set is a mapping table defining logical-to-physical memory address translations.

17. (Currently amended) The data processing system of claim 15, further comprising a set of instructions that is executed by the processor, wherein the set of instructions provides logical partitioning management.

18. (Currently amended) The data processing system of claim 15, further comprising a mapping table that defines logical-to-physical memory address translations, the mapping table ~~wherein the data set~~

~~is~~ maintained in the memory in at least one of the first and second ranges of contiguous physical addresses. ~~physical address ranges~~.

19. (Currently amended) The data processing system of claim 15, further comprising a set of instructions that is executed by the processor for virtualizing the first, second, and third ranges of contiguous physical addresses, wherein the set of instructions is [[are]] maintained in the memory in at least one of the first and second ranges of contiguous physical addresses. ~~physical address ranges.~~

20. (Currently amended) The data processing system of claim 15, further comprising:

the combined range of contiguous logical addresses being non-contiguous with the third range of contiguous logical addresses.

~~wherein a second logical address range is mapped to the third physical address range, and a lower most logical address of the second logical address range is greater than an upper most logical address of the contiguous logical address range.~~

REMARKS/ARGUMENTS

Amendments were made to the specification to correct errors and to clarify the specification. No new matter has been added by any of the amendments to the specification.

Claims 1-20 are pending in the present application. With this amendment, claims 1 and 7-20 have been amended. Reconsideration of the claims is respectfully requested.

I. Interview Summary

Applicant thanks the Examiner and her Supervisor for the courtesies extended in the interview that was held on July 12, 2006. An agreement was not reached during the interview.

An Interview Summary was mailed July 18, 2006. In it, the Examiner notes that Applicant and the Examiner discussed figure 19 of *Harvey* and the "correspondence of physical addresses in figure 19 to non-contiguous physical addresses specified in claim 1". With all due respect to the Examiner, the Interview Summary is inaccurate. Applicant did not discuss the correspondence of physical addresses in figure 19. Applicant discussed figure 19 of *Harvey* and its depiction of virtual addresses, not physical addresses. Applicant described figure 19 as depicting virtual addresses. Applicant also described the differences between the virtual addresses depicted in figure 19 and the physical address ranges and logical address ranges that are described in Applicant's claim 1.

II. Objections to the Claims

The Examiner objected to claims 1 and 7 because of informalities.

Applicant has amended claim 1 merely to correct the typographical error that was noted by the Examiner and not in response to any prior art cited by the Examiner.

Applicant has amended claim 7. The informalities noted by the Examiner have been amended.

Because Applicant's claims have been amended to correct the typographical errors that were noted by the Examiner, this objection has been overcome and should be withdrawn.

III. 35 U.S.C. § 101

The Examiner has rejected claims 7-14 under 35 U.S.C. § 101 as being directed towards non-statutory subject matter. Specifically, the Examiner stated that the claims recite the limitation of a computer readable medium that Applicant's specification defines as transmission-type media.

Applicant has amended the specification to remove language directed to transmission-type media. Applicant has also amended claim 7 to recite "A computer program product that is stored in a computer readable medium". Therefore, this rejection has been overcome and should be withdrawn.

IV. 35 U.S.C. § 103(a)

The Examiner has rejected claims 1-5, 7-13, 15-20 under 35 U.S.C. § 103(a) as being unpatentable over *Harvey* (US 6,061,773) in view of *Stine* (US 6,629,111). This rejection, as it might be applied to claims 1-5 and to claims 7-13, and 15-20 as amended, is respectfully traversed.

Applicant's independent claim 1 describes virtualizing a first physical address range to produce a first logical address range. A second physical address range is virtualized to produce a second logical address range. A memory mapped input/output (MMIO) physical address range is intermediate the first and second physical address ranges. The first and second physical address ranges are non-contiguous. The first and second logical address ranges are contiguous. The MMIO physical address range is virtualized to produce a third logical address range. A lowermost logical address of the third logical address range exceeds a respective uppermost logical address of the first and second logical address ranges.

Harvey teaches a virtual memory system. The virtual address space is divided into a shared address space, which is accessible by any process, a process private space, which is accessible only by a specific process, and a page table space that is located between the process private space and the shared space. These three different spaces, shared, process private, and page table space are all part of the virtual address space.

A page table includes page table entries. Each page table entry maps a single virtual page to a single physical page. An exemplary page table entry is shown in Figure 2. It includes page frame numbers. The page frame number is a physical address that specifies a page of physical memory. Thus, the virtual page that the page table entry represents is mapped to the physical page whose address is stored in that page table entry.

Harvey teaches a new virtual memory system whereby the page table space can be adjacent to the process private space and the shared space. The process private space, shared space, and page table spaces are in the virtual memory space. The page table space may include a set of virtually contiguous shared page table entries adjacent to the shared space and a set of virtually contiguous process private page table entries adjacent to the process private space. These virtually contiguous entries are in the virtual memory space. Although *Harvey* teaches virtually contiguous page table entries that are in the virtual address space, *Harvey* does not teach that the physical pages associated with these entries are contiguous.

In contradistinction, Applicant's claim 1 recites a first physical address range and a second physical address range that are non-contiguous. A memory mapped input/output physical address range

is intermediate the first and second physical address ranges. These are ranges of physical addresses, not virtual addresses.

Applicant also claims virtualizing the first physical address range to produce a first logical address range and virtualizing the second physical address range to produce a second logical address range. The first logical address range and the second logical address range are contiguous. These are ranges of logical addresses, not physical addresses.

The memory mapped input/output physical address range is virtualized to produce a third logical address range. A lowermost logical address of the third logical address range exceeds a respective uppermost logical address of the first and second logical address ranges.

Thus, two non-contiguous physical address ranges are virtualized to produce two contiguous logical address ranges. In addition, a physical address range that is intermediate the two non-contiguous physical address ranges is virtualized to produce a third logical address range that has a lowermost logical address that exceeds an uppermost logical address of the non-contiguous physical address ranges.

Harvey does not teach or suggest a range of physical addresses. In *Harvey*, each page table entry is associated with a virtual address. A physical address is stored in the page table entry. *Harvey* also teaches a set of virtually contiguous page table entries, each of which represents a virtual page, that is in the virtual space; thus, *Harvey* teaches virtually contiguous virtual pages. *Harvey* does not, however, teach a range of physical addresses.

Harvey does not teach the set of virtually contiguous page table entries being associated with a range of physical addresses. For example, Figure 4 of *Harvey* depicts virtual page 1 being associated with page table entry 1 (PTE 1), virtual page 2 being associated with page table entry 2 (PTE 2), virtual page 3 being associated with page table entry 3 (PTE 3), and so on. A physical address is stored in page table entry 1 (PTE 1), another physical address is stored in page table entry 2 (PTE 2), and another physical address is stored in PTE 3. *Harvey* does not teach that the physical address stored in PTE 1, the physical address that is stored in PTE 2, and the physical address that is stored in PTE 3 are contiguous. Therefore, *Harvey* does not teach a range of physical addresses.

Harvey also does not teach or suggest virtualizing two ranges of non-contiguous physical addresses to produce two ranges of logical addresses that are contiguous.

Harvey does not teach or suggest virtualizing a memory mapped input/output physical address range that is intermediate the first and second physical address ranges to produce a third logical address range.

Harvey does not teach or suggest virtualizing a memory mapped input/output physical address range that is intermediate the first and second physical address ranges to produce a third logical address

range where a lowermost logical address of the third logical address range exceeds a respective uppermost logical address of the first and second logical address ranges.

The Examiner refers to figure 19 of *Harvey* and its associated text in column 22, lines 60-66. Figure 19 depicts a virtual address space 450. Virtual address space 450 is not a range of physical addresses. Figure 19 does not depict physical addresses.

Virtual address space 450 is divided into three parts, which includes an inaccessible gap 456. *Harvey* does not teach how the three virtual address parts of virtual address space are produced. Applicant does claim three logical address ranges; however, these logical address ranges are produced by virtualizing physical address ranges as described above. First and second non-contiguous physical address ranges are virtualized to produce first and second logical ranges that are contiguous. A physical address range that is intermediate the first and second physical address ranges is virtualized to produce a third logical address range. A lowermost logical address of the third logical address range exceeds a respective uppermost logical address of the first and second logical address range.

Harvey does not teach or suggest two non-contiguous physical address ranges that are virtualized to product two contiguous logical address ranges. *Harvey* does not teach or suggest a physical address range that is intermediate the two non-contiguous physical ranges being virtualized to produce a third logical range where a lowermost logical address of the third logical address range exceeds a respective uppermost logical address of the two physical address ranges.

Applicant's independent claims 7 and 15 describe similar features. These claims describe virtualizing a first range of contiguous physical addresses to produce a first range of contiguous logical addresses. A second range of contiguous physical addresses is virtualized to produce a second range of contiguous logical addresses. The first and second ranges of contiguous physical addresses are non-contiguous. The first and second ranges of contiguous logical addresses are contiguous and form a combined range of contiguous logical addresses.

A third range of contiguous physical addresses is virtualized to produce a third range of contiguous logical addresses. The third range of contiguous physical addresses is intermediate to the first and second ranges of contiguous physical addresses. A lowermost logical address of the third range of contiguous logical addresses exceeds an uppermost logical address of the combined range of contiguous logical addresses.

Harvey does not teach or suggest a range of contiguous physical addresses, a first and second range of contiguous physical addresses that are non-contiguous, a first and second range of contiguous physical addresses that are non-contiguous that virtualized to produce a first and second range of contiguous logical addresses that are contiguous and that form a combined range of contiguous logical addresses, a third range of contiguous physical addresses that is intermediate to the first and second

ranges of contiguous physical addresses, a third range of contiguous physical addresses that are virtualized to produce a third range of contiguous logical addresses where the lowermost logical address of the third range of contiguous logical addresses exceeds an uppermost logical address of the combined range of contiguous logical addresses.

The Examiner relies on *Stine* to cure the deficiencies of *Harvey*. Because *Stine* does not cure the deficiencies discussed above, the combination of *Harvey* and *Stine* does not render Applicant's claims obvious.

The remaining claims depend from the independent claims discussed above; therefore, the remaining claims are patentable for the reasons given above.

The Examiner has rejected claims 6 and 14 under 35 U.S.C. § 103(a) over *Harvey*, in view of *Stine*, as applied to claims 1-5, 7-13, 15-20 and further in view of *Yazdy*. This rejection, as it might be applied to claim 6 and to claim 14 as amended, is respectfully traversed.

Since claims 6 and 14 depend from Applicant's independent claims discussed above, the same distinctions between the combination of *Harvey* and *Stine* and Applicant's independent claims discussed above apply for claims 6 and 14. *Yazdy* does not make up for the deficiencies discussed above. Therefore, this rejection has been overcome and should be withdrawn.

V. Conclusion

It is respectfully urged that the subject application is patentable over the cited prior art and is now in condition for allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: August 2, 2006

Respectfully submitted,

/Lisa L.B. Yociss/

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